PRELIMINARY PRODUCT SPECIFICATION

SHARP

Integrated Circuits Group

# LH28F128BFHT-PBTL75A

## Flash Memory
## 16Mbit (8Mbitx16)

(Model Number: LHF12F17)

Spec. Issue Date: June 7, 2004

SHARP

| SPEC No. | FM046012 |
|---|---|
| ISSUE: | Jun. 7, 2004 |

To; _____

PRELIMINARY

# SPECIFICATIONS

Product Type 128Mbit Flash Memory

## LH28F128BFHT—PBTL75A

Model No. (LHF12F17)

This device specification is subject to change without notice.

* This specifications contains 32 pages including the cover and appendix.

CUSTOMERS ACCEPTANCE

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

# CONTENTS

# LH28F128BFHT-PBTL75A
# 128Mbit (8Mbit×16)
# Page Mode Dual Work Flash MEMORY

■ 128-M density with 16-bit I/O Interface

■ High Performance Reads
- 75/25ns 8-Word Page Mode

■ 6-Plane Dual Work Operation
- Read operations are available during Block Erase or (Page Buffer) Program between two different Planes
- Plane Architecture: 16M, 24M, 24M, 24M, 24M, 16M

■ Low Power Operation
- 2.7V Read and Write Operations
- $V_{CCQ}$ for Input/Output Power Supply Isolation
- Automatic Power Savings Mode reduces $I_{CCR}$ in Static Mode

■ Enhanced Code + Data Storage
- 5µs Typical Erase/Program Suspends

■ OTP (One Time Program) Block
- 4-Word Factory-Programmed Area
- 4-Word User-Programmable Area

■ High Performance Program with Page Buffer
- 16-Word Page Buffer
- 5µs/Word (Typ.) at WP#/ACC=9.5V

■ Operating Temperature -40°C to +85°C

■ CMOS Process (P-type silicon substrate)

■ Flexible Blocking Architecture
- Eight 4-Kword Parameter Blocks
- Two-hundred and fifty-five 32-Kword Main Blocks
- Bottom Parameter Location

■ Enhanced Data Protection Features
- Individual Block Lock and Block Lock-Down with Zero-Latency
- All blocks are locked at power-up or device reset.
- Block Erase, Full Chip Erase, (Page Buffer) Word Program Lockout during Power Transitions

■ Automated Erase/Program Algorithms
- 3.0V Low-Power 11µs/Word (Typ.) Programming
- 9.5V No Glue Logic 9µs/Word (Typ.) Production Programming and 0.8s Erase (Typ.)

■ Cross-Compatible Command Support
- Basic Command Set
- Common Flash Interface (CFI)

■ Extended Cycling Capability
- Minimum 100,000 Block Erase Cycles

■ 56-Lead TSOP (Normal Bend)

■ ETOX$^{TM*}$ Flash Technology

■ Not designed or rated as radiation hardened

The product, which is 6-Plane Page Mode Dual Work (Simultaneous Read while Erase/Program) Flash memory, is a low power, high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at $V_{CC}$=2.7V-3.3V. Its low voltage operation capability greatly extends battery life for portable applications.

The product provides high performance asynchronous page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states.

The memory array block architecture utilizes Enhanced Data Protection features, and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program.

Special OTP (One Time Program) block provides an area to store permanent code such as an unique number.

* ETOX is a trademark of Intel Corporation.

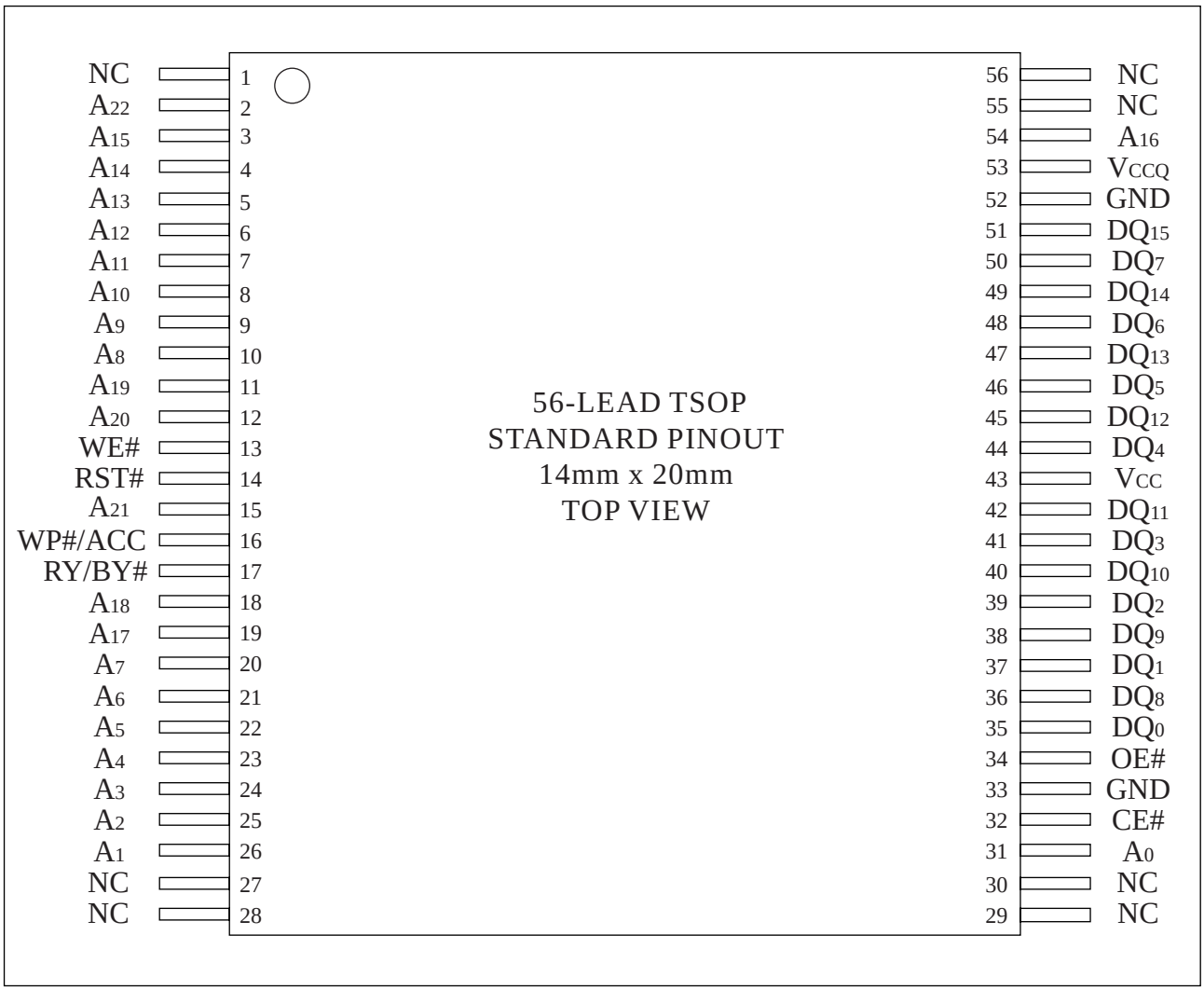



Figure 1. 56-Lead TSOP (Normal Bend) Pinout

Table 1. Pin Descriptions

| Symbol | Type | Name and Function |
|---|---|---|
| $A_{22}$-$A_0$ | INPUT | ADDRESS INPUTS: Inputs for addresses. |
| $DQ_{15}$-$DQ_0$ | INPUT/ OUTPUT | DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code and identifier code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle. |
| CE# | INPUT | CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high ($V_{IH}$) deselects the device and reduces power consumption to standby levels. |
| RST# | INPUT | RESET: When low ($V_{IL}$), RST# resets internal automation and inhibits write operations which provides data protection. RST#-high ($V_{IH}$) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RST# must be low during power-up/down. |
| OE# | INPUT | OUTPUT ENABLE: Gates the device's outputs during a read cycle. |
| WE# | INPUT | WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of CE# or WE# (whichever goes high first). |
| WP#/ACC | INPUT/ SUPPLY | WRITE PROTECT: When WP#/ACC is $V_{IL}$, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and not locked-down. When WP#/ACC is $V_{IH}$, lock-down is disabled.<br>Applying 9.5V±0.5V to WP#/ACC provides fast erasing or fast programming mode. In this mode, WP#/ACC is power supply pin. Applying 9.5V±0.5V to WP#/ACC during erase/program can only be done for a maximum of 1,000 cycles on each block. WP#/ ACC may be connected to 9.5V±0.5V for a total of 80 hours maximum. Use of this pin at 9.5V+0.5V beyond these limits may reduce block cycling capability or cause permanent damage. |
| RY/BY# | OPEN DRAIN OUTPUT | READY/BUSY#: Indicates the status of the internal WSM (Write State Machine). When low, WSM is performing an internal operation (block erase, full chip erase, (page buffer) program or OTP program). RY/BY#-High Z indicates that the WSM is ready for new commands, block erase is suspended and (page buffer) program is inactive, (page buffer) program is suspended, or the device is in reset mode. |
| $V_{CC}$ | SUPPLY | DEVICE POWER SUPPLY (2.7V-3.3V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid $V_{CC}$ voltage (see DC Characteristics) produce spurious results and should not be attempted. |
| $V_{CCQ}$ | SUPPLY | INPUT/OUTPUT POWER SUPPLY (2.7V-3.3V): Power supply for all input/output pins. |
| GND | SUPPLY | GROUND: Do not float any ground pins. |
| NC | | NO CONNECT: Lead is not internally connected; it may be driven or floated. |

Table 2. Simultaneous Operation Modes Allowed with 6 Planes [1, 2]

| IF ONE PLANE IS: | THEN THE MODES ALLOWED IN THE OTHER PLANE IS: | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Read Array | Read ID/OTP | Read Status | Read Query | Word Program | Page Buffer Program | OTP Program | Block Erase | Full Chip Erase | Program Suspend | Block Erase Suspend |
| Read Array | X | X | X | X | X | X | | X | | X | X |
| Read ID/OTP | X | X | X | X | X | X | | X | | X | X |
| Read Status | X | X | X | X | X | X | X | X | X | X | X |
| Read Query | X | X | X | X | X | X | | X | | X | X |
| Word Program | X | X | X | X | | | | | | | X |
| Page Buffer Program | X | X | X | X | | | | | | | X |
| OTP Program | | | X | | | | | | | | |
| Block Erase | X | X | X | X | | | | | | | |
| Full Chip Erase | | | X | | | | | | | | |
| Program Suspend | X | X | X | X | | | | | | | X |
| Block Erase Suspend | X | X | X | X | X | X | | | | X | |

NOTES:
1. "X" denotes the operation available.
2. Dual Work Restrictions:
   Status register reflects WSM (Write State Machine) state.
   Only one plane can be erased or programmed at a time - no command queuing.
   Commands must be written to an address within the block targeted by that command.

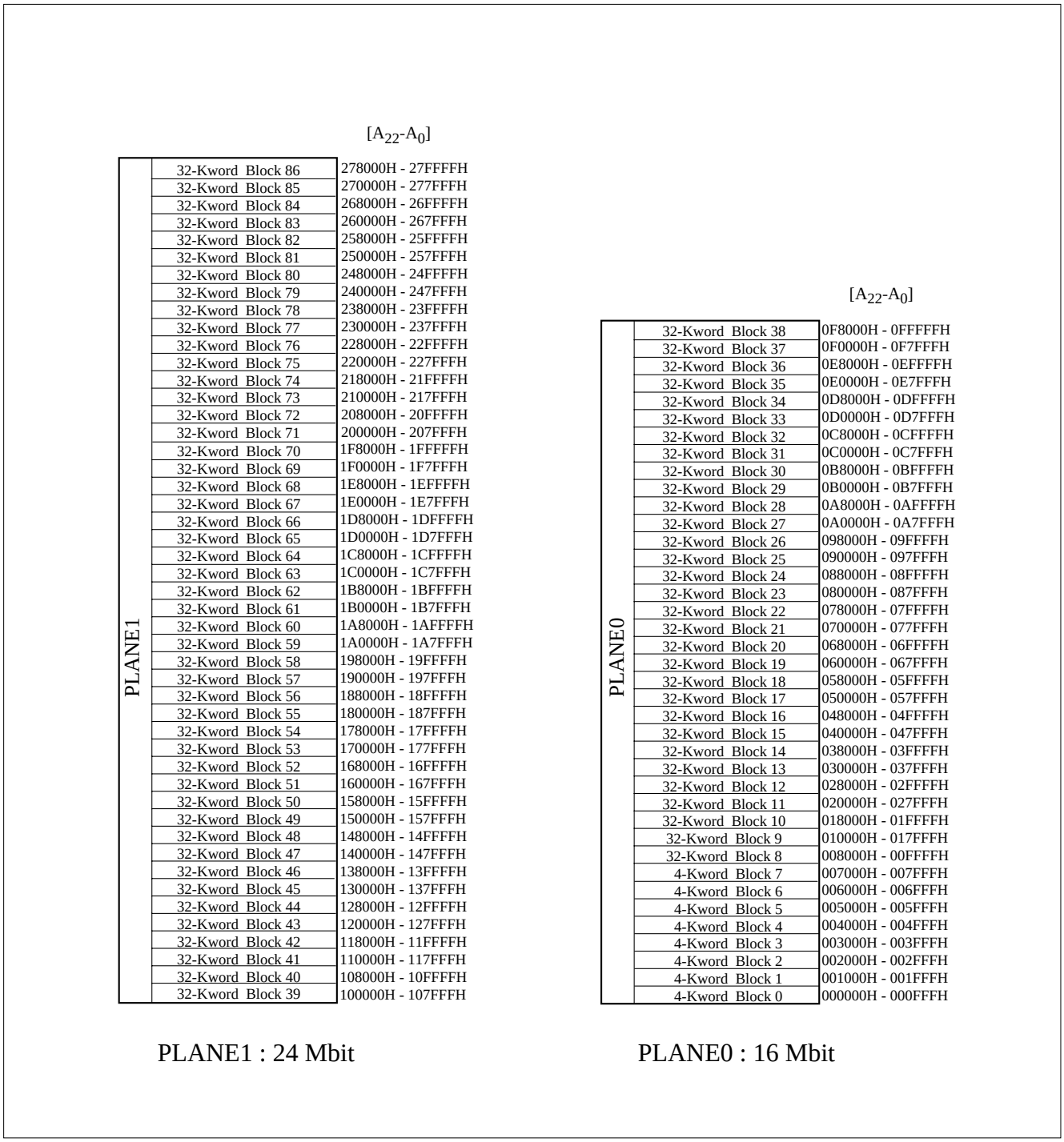



Figure 2.1. Memory Map (Bottom Parameter, Plane 0 and Plane 1)

| | | [$A_{22}$-$A_0$] |
|---|---|---|
| PLANE3 | 32-Kword Block 182 | 578000H - 57FFFFH |
| | 32-Kword Block 181 | 570000H - 577FFFH |
| | 32-Kword Block 180 | 568000H - 56FFFFH |
| | 32-Kword Block 179 | 560000H - 567FFFH |
| | 32-Kword Block 178 | 558000H - 55FFFFH |
| | 32-Kword Block 177 | 550000H - 557FFFH |
| | 32-Kword Block 176 | 548000H - 54FFFFH |
| | 32-Kword Block 175 | 540000H - 547FFFH |
| | 32-Kword Block 174 | 538000H - 53FFFFH |
| | 32-Kword Block 173 | 530000H - 537FFFH |
| | 32-Kword Block 172 | 528000H - 52FFFFH |
| | 32-Kword Block 171 | 520000H - 527FFFH |
| | 32-Kword Block 170 | 518000H - 51FFFFH |
| | 32-Kword Block 169 | 510000H - 517FFFH |
| | 32-Kword Block 168 | 508000H - 50FFFFH |
| | 32-Kword Block 167 | 500000H - 507FFFH |
| | 32-Kword Block 166 | 4F8000H - 4FFFFFH |
| | 32-Kword Block 165 | 4F0000H - 4F7FFFH |
| | 32-Kword Block 164 | 4E8000H - 4EFFFFH |
| | 32-Kword Block 163 | 4E0000H - 4E7FFFH |
| | 32-Kword Block 162 | 4D8000H - 4DFFFFH |
| | 32-Kword Block 161 | 4D0000H - 4D7FFFH |
| | 32-Kword Block 160 | 4C8000H - 4CFFFFH |
| | 32-Kword Block 159 | 4C0000H - 4C7FFFH |
| | 32-Kword Block 158 | 4B8000H - 4BFFFFH |
| | 32-Kword Block 157 | 4B0000H - 4B7FFFH |
| | 32-Kword Block 156 | 4A8000H - 4AFFFFH |
| | 32-Kword Block 155 | 4A0000H - 4A7FFFH |
| | 32-Kword Block 154 | 498000H - 49FFFFH |
| | 32-Kword Block 153 | 490000H - 497FFFH |
| | 32-Kword Block 152 | 488000H - 48FFFFH |
| | 32-Kword Block 151 | 480000H - 487FFFH |
| | 32-Kword Block 150 | 478000H - 47FFFFH |
| | 32-Kword Block 149 | 470000H - 477FFFH |
| | 32-Kword Block 148 | 468000H - 46FFFFH |
| | 32-Kword Block 147 | 460000H - 467FFFH |
| | 32-Kword Block 146 | 458000H - 45FFFFH |
| | 32-Kword Block 145 | 450000H - 457FFFH |
| | 32-Kword Block 144 | 448000H - 44FFFFH |
| | 32-Kword Block 143 | 440000H - 447FFFH |
| | 32-Kword Block 142 | 438000H - 43FFFFH |
| | 32-Kword Block 141 | 430000H - 437FFFH |
| | 32-Kword Block 140 | 428000H - 42FFFFH |
| | 32-Kword Block 139 | 420000H - 427FFFH |
| | 32-Kword Block 138 | 418000H - 41FFFFH |
| | 32-Kword Block 137 | 410000H - 417FFFH |
| | 32-Kword Block 136 | 408000H - 40FFFFH |
| | 32-Kword Block 135 | 400000H - 407FFFH |

PLANE3 : 24 Mbit

| | | [$A_{22}$-$A_0$] |
|---|---|---|
| PLANE2 | 32-Kword Block 134 | 3F8000H - 3FFFFFH |
| | 32-Kword Block 133 | 3F0000H - 3F7FFFH |
| | 32-Kword Block 132 | 3E8000H - 3EFFFFH |
| | 32-Kword Block 131 | 3E0000H - 3E7FFFH |
| | 32-Kword Block 130 | 3D8000H - 3DFFFFH |
| | 32-Kword Block 129 | 3D0000H - 3D7FFFH |
| | 32-Kword Block 128 | 3C8000H - 3CFFFFH |
| | 32-Kword Block 127 | 3C0000H - 3C7FFFH |
| | 32-Kword Block 126 | 3B8000H - 3BFFFFH |
| | 32-Kword Block 125 | 3B0000H - 3B7FFFH |
| | 32-Kword Block 124 | 3A8000H - 3AFFFFH |
| | 32-Kword Block 123 | 3A0000H - 3A7FFFH |
| | 32-Kword Block 122 | 398000H - 39FFFFH |
| | 32-Kword Block 121 | 390000H - 397FFFH |
| | 32-Kword Block 120 | 388000H - 38FFFFH |
| | 32-Kword Block 119 | 380000H - 387FFFH |
| | 32-Kword Block 118 | 378000H - 37FFFFH |
| | 32-Kword Block 117 | 370000H - 377FFFH |
| | 32-Kword Block 116 | 368000H - 36FFFFH |
| | 32-Kword Block 115 | 360000H - 367FFFH |
| | 32-Kword Block 114 | 358000H - 35FFFFH |
| | 32-Kword Block 113 | 350000H - 357FFFH |
| | 32-Kword Block 112 | 348000H - 34FFFFH |
| | 32-Kword Block 111 | 340000H - 347FFFH |
| | 32-Kword Block 110 | 338000H - 33FFFFH |
| | 32-Kword Block 109 | 330000H - 337FFFH |
| | 32-Kword Block 108 | 328000H - 32FFFFH |
| | 32-Kword Block 107 | 320000H - 327FFFH |
| | 32-Kword Block 106 | 318000H - 31FFFFH |
| | 32-Kword Block 105 | 310000H - 317FFFH |
| | 32-Kword Block 104 | 308000H - 30FFFFH |
| | 32-Kword Block 103 | 300000H - 307FFFH |
| | 32-Kword Block 102 | 2F8000H - 2FFFFFH |
| | 32-Kword Block 101 | 2F0000H - 2F7FFFH |
| | 32-Kword Block 100 | 2E8000H - 2EFFFFH |
| | 32-Kword Block 99 | 2E0000H - 2E7FFFH |
| | 32-Kword Block 98 | 2D8000H - 2DFFFFH |
| | 32-Kword Block 97 | 2D0000H - 2D7FFFH |
| | 32-Kword Block 96 | 2C8000H - 2CFFFFH |
| | 32-Kword Block 95 | 2C0000H - 2C7FFFH |
| | 32-Kword Block 94 | 2B8000H - 2BFFFFH |
| | 32-Kword Block 93 | 2B0000H - 2B7FFFH |
| | 32-Kword Block 92 | 2A8000H - 2AFFFFH |
| | 32-Kword Block 91 | 2A0000H - 2A7FFFH |
| | 32-Kword Block 90 | 298000H - 29FFFFH |
| | 32-Kword Block 89 | 290000H - 297FFFH |
| | 32-Kword Block 88 | 288000H - 28FFFFH |
| | 32-Kword Block 87 | 280000H - 287FFFH |

PLANE2 : 24 Mbit

Figure 2.2. Memory Map (Bottom Parameter, Plane 2 and Plane 3)

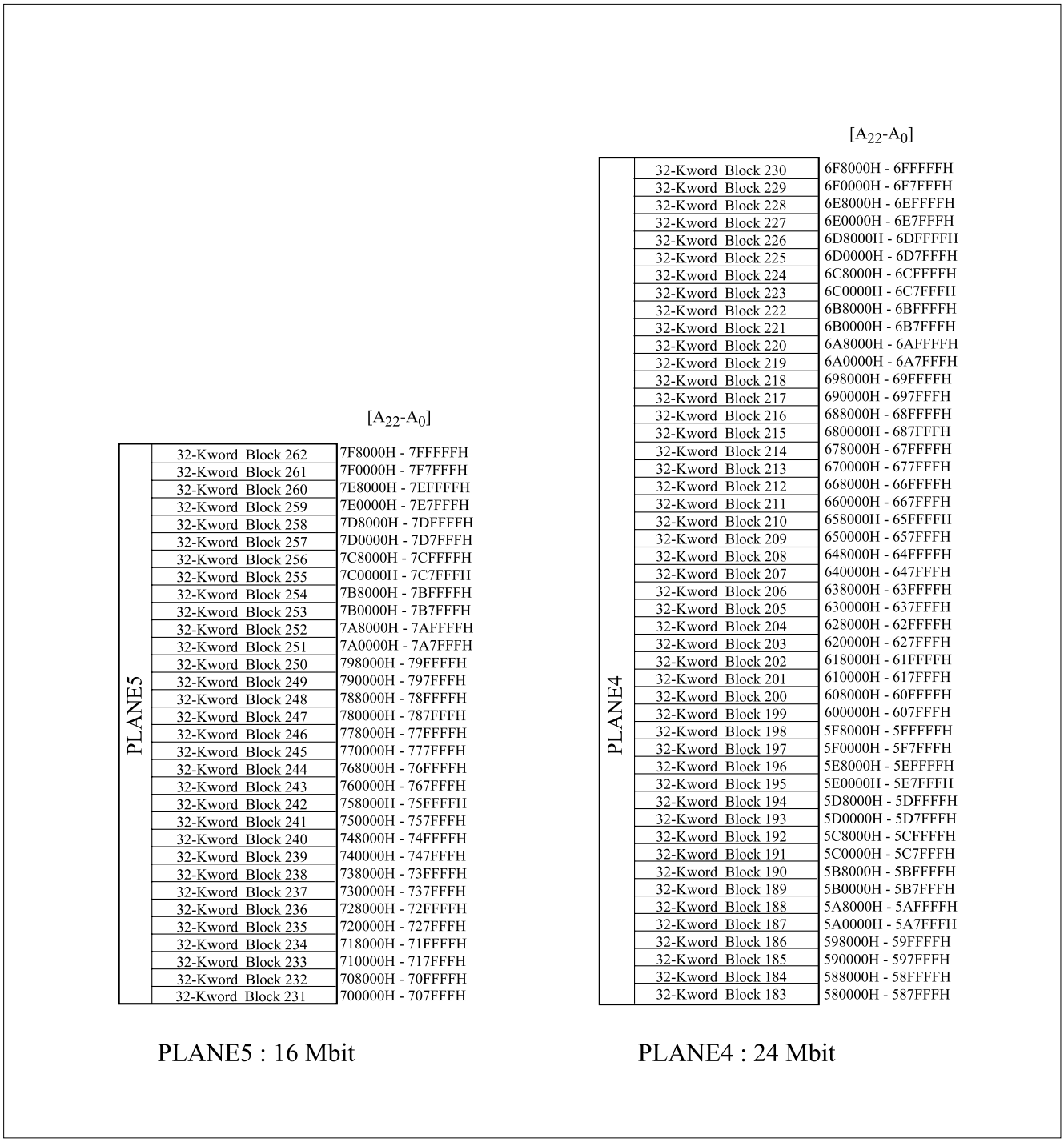



Figure 2.3. Memory Map (Bottom Parameter, Plane 4 and Plane 5)

Table 3. Identifier Codes and OTP Address for Read Operation

| | Code | Address [$A_{15}$-$A_0$] | Data [$DQ_{15}$-$DQ_0$] | Notes |
|---|---|---|---|---|
| Manufacturer Code | Manufacturer Code | 0000H | 00B0H | 1 |
| Device Code | Device Code | 0001H | 0011H | 1 |
| Block Lock Configuration Code | Block is Unlocked | Block Address + 2 | $DQ_0$ = 0 | 2, 3 |
| | Block is Locked | | $DQ_0$ = 1 | 2, 3 |
| | Block is not Locked-Down | | $DQ_1$ = 0 | 2, 3 |
| | Block is Locked-Down | | $DQ_1$ = 1 | 2, 3 |
| OTP | OTP Lock | 0080H | OTP-LK | 1, 4 |
| | OTP | 0081-0088H | OTP | 1, 5 |

NOTES:
1. $A_{22}$-$A_{16}$ must be the address within the plane to which the Read Identifier Codes/OTP command (90H) has been written.
2. Block Address = The beginning location of a block address within the plane to which the Read Identifier Codes/OTP command (90H) has been written.
3. $DQ_{15}$-$DQ_2$ are reserved for future implementation.
4. OTP-LK=OTP Block Lock configuration.
5. OTP=OTP Block data.

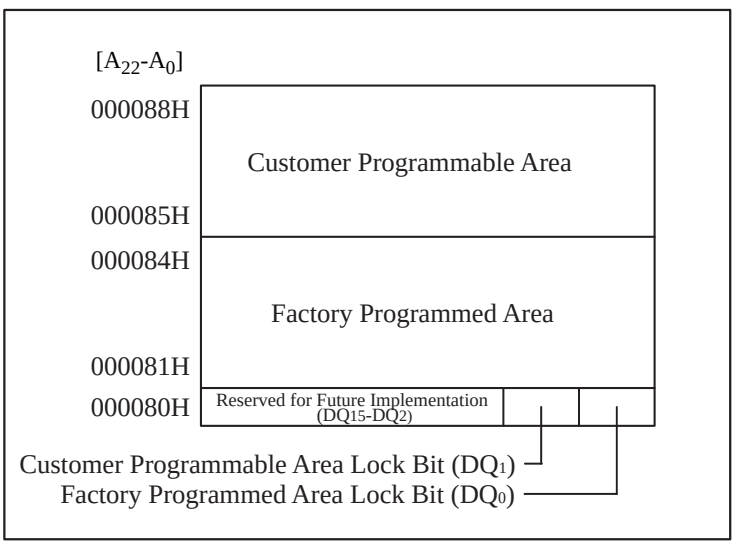



Figure 3. OTP Block Address Map for OTP Program
(The area outside 80H~88H cannot be used.)

Table 4. Bus Operation[1, 2]

| Mode | Notes | RST# | CE# | OE# | WE# | Address | $DQ_{15-0}$ | RY/BY# [8] |
|---|---|---|---|---|---|---|---|---|
| Read Array | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $D_{OUT}$ | High Z |
| Output Disable | | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | High Z | X |
| Standby | | $V_{IH}$ | $V_{IH}$ | X | X | X | High Z | X |
| Reset | 3 | $V_{IL}$ | X | X | X | X | High Z | High Z |
| Read Identifier Codes/OTP | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | See Table 3 | See Table 3 | High Z |
| Read Query | 6,7 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $D_{OUT}$ | High Z |
| Read Status Register | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $D_{OUT}$ | X |
| Write | 4,5,6 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | $D_{IN}$ | X |

NOTES:
1. Refer to DC Characteristics for $V_{IL}$ or $V_{IH}$ voltages.
2. X can be $V_{IL}$ or $V_{IH}$ for control pins and addresses.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving block erase, full chip erase, (page buffer) program or OTP program are reliably executed when $V_{CC}$=2.7V-3.3V.
5. Refer to Table 5 for valid $D_{IN}$ during a write operation.
6. Never hold OE# low and WE# low at the same timing.
7. Query code = Common Flash Interface (CFI) code.
8. RY/BY# is $V_{OL}$ when the WSM (Write State Machine) is executing internal block erase, full chip erase, (page buffer) program or OTP program algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with program and page buffer program inactive), (page buffer) program suspend mode, or reset mode.

Table 5. Command Definitions(11)

| Command | Bus Cycles Req'd | Notes | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|---|
| | | | Oper(1) | Addr(2) | Data | Oper(1) | Addr(2) | Data(3) |
| Read Array | 1 | | Write | PA | FFH | | | |
| Read Identifier Codes/OTP | ≥ 2 | 4 | Write | PA | 90H | Read | IA or OA | ID or OD |
| Read Query | ≥ 2 | 4 | Write | PA | 98H | Read | QA | QD |
| Read Status Register | 2 | | Write | PA | 70H | Read | PA | SRD |
| Clear Status Register | 1 | | Write | PA | 50H | | | |
| Block Erase | 2 | 5 | Write | BA | 20H | Write | BA | D0H |
| Full Chip Erase | 2 | 5,9 | Write | X | 30H | Write | X | D0H |
| Program | 2 | 5,6 | Write | WA | 40H or 10H | Write | WA | WD |
| Page Buffer Program | ≥ 4 | 5,7 | Write | WA | E8H | Write | WA | N-1 |
| Block Erase and (Page Buffer) Program Suspend | 1 | 8,9 | Write | PA | B0H | | | |
| Block Erase and (Page Buffer) Program Resume | 1 | 8,9 | Write | PA | D0H | | | |
| Set Block Lock Bit | 2 | | Write | BA | 60H | Write | BA | 01H |
| Clear Block Lock Bit | 2 | 10 | Write | BA | 60H | Write | BA | D0H |
| Set Block Lock-down Bit | 2 | | Write | BA | 60H | Write | BA | 2FH |
| OTP Program | 2 | 9 | Write | OA | C0H | Write | OA | OD |

NOTES:
1. Bus operations are defined in Table 4.
2. All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.
   X=Any valid address within the device.
   PA=Address within the selected plane.
   IA=Identifier codes address (See Table 3).
   QA=Query codes address.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
   OA=Address of OTP block to be read or programmed (See Figure 3).
3. ID=Data read from identifier codes. (See Table 3).
   QD=Data read from query database.
   SRD=Data read from status register. See Table 9.1, Table 9.2 for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.
   OD=Data within OTP block. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.
   N-1=N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code and the data within OTP block (See Table 3).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is $V_{IH}$.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.

7. Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H).
8. If the program operation in one plane is suspended and the erase operation in other plane is also suspended, the suspended program operation will be resumed first.
9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP#/ACC is $V_{IL}$. When WP#/ACC is $V_{IH}$, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 6. Functions of Block Lock[5] and Block Lock-Down

| Current State | | | | | Erase/Program Allowed [2] |
|---|---|---|---|---|---|
| State | WP#/ACC | $DQ_1$[1] | $DQ_0$[1] | State Name | |
| [000] | 0 | 0 | 0 | Unlocked | Yes |
| [001][3] | 0 | 0 | 1 | Locked | No |
| [011] | 0 | 1 | 1 | Locked-down | No |
| [100] | 1 | 0 | 0 | Unlocked | Yes |
| [101][3] | 1 | 0 | 1 | Locked | No |
| [110][4] | 1 | 1 | 0 | Lock-down Disable | Yes |
| [111] | 1 | 1 | 1 | Lock-down Disable | No |

NOTES:
1. $DQ_0$=1: a block is locked; $DQ_0$=0: a block is unlocked.
   $DQ_1$=1: a block is locked-down; $DQ_1$=0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (WP#/ACC=0) or [101] (WP#/ACC=1), regardless of the states before power-off or reset operation.
4. When WP#/ACC is driven to $V_{IL}$ in [110] state, the state changes to [011] and the blocks are automatically locked.
5. OTP (One Time Program) block has the lock function which is different from those described above.

Table 7. Block Locking State Transitions upon Command Write[4]

| Current State | | | | Result after Lock Command Written (Next State) | | |
|---|---|---|---|---|---|---|
| State | WP#/ACC | $DQ_1$ | $DQ_0$ | Set Lock[1] | Clear Lock[1] | Set Lock-down[1] |
| [000] | 0 | 0 | 0 | [001] | No Change | [011][2] |
| [001] | 0 | 0 | 1 | No Change[3] | [000] | [011] |
| [011] | 0 | 1 | 1 | No Change | No Change | No Change |
| [100] | 1 | 0 | 0 | [101] | No Change | [111][2] |
| [101] | 1 | 0 | 1 | No Change | [100] | [111] |
| [110] | 1 | 1 | 0 | [111] | No Change | [111][2] |
| [111] | 1 | 1 | 1 | No Change | [110] | No Change |

NOTES:
1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block ($DQ_0$=0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that WP#/ACC is not changed and fixed $V_{IL}$ or $V_{IH}$.

Table 8. Block Locking State Transitions upon WP#/ACC Transition[4]

| Previous State | Current State | | | | Result after WP#/ACC Transition (Next State) | |
|---|---|---|---|---|---|---|
| | State | WP#/ACC | $DQ_1$ | $DQ_0$ | WP#/ACC=0→1[1] | WP#/ACC=1→0[1] |
| - | [000] | 0 | 0 | 0 | [100] | - |
| - | [001] | 0 | 0 | 1 | [101] | - |
| [110][2] | [011] | 0 | 1 | 1 | [110] | - |
| Other than [110][2] | | | | | [111] | - |
| - | [100] | 1 | 0 | 0 | - | [000] |
| - | [101] | 1 | 0 | 1 | - | [001] |
| - | [110] | 1 | 1 | 0 | - | [011][3] |
| - | [111] | 1 | 1 | 1 | - | [011] |

NOTES:
1. "WP#/ACC=0→1" means that WP#/ACC is driven to $V_{IH}$ and "WP#/ACC=1→0" means that WP#/ACC is driven to $V_{IL}$.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When WP#/ACC is driven to $V_{IL}$ in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

Table 9.1. Status Register Definition

| GWSMS | GBESS | GBEFCES | GPBPOPS | GWPACCS | GPBPSS | GDPS | R |
|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PWSMS | GBESS | GBEFCES | GPBPOPS | GWPACCS | GPBPSS | GDPS | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| | NOTES: |
|---|---|
| SR.7 = PLANE WRITE STATE MACHINE STATUS (PWSMS)<br>1 = Ready<br>0 = Busy | Status Register indicates the status of the WSM (Write State Machine). However, SR.7 indicates the status of WSM in each plane. Even if the SR.7 is "1", the WSM may be occupied by the other plane. |
| SR.6 = GLOBAL BLOCK ERASE SUSPEND STATUS (GBESS)<br>1 = Block Erase Suspended<br>0 = Block Erase in Progress/Completed | In the plane to which the command is issued, Check SR.7 or RY/BY# to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0". |
| SR.5 = GLOBAL BLOCK ERASE AND FULL CHIP ERASE STATUS (GBEFCES)<br>1 = Error in Block Erase or Full Chip Erase<br>0 = Successful Block Erase or Full Chip Erase | If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit attempt, an improper command sequence was entered. |
| SR.4 = GLOBAL (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (GPBPOPS)<br>1 = Error in (Page Buffer) Program or OTP Program<br>0 = Successful (Page Buffer) Program or OTP Program | |
| SR.3 = GLOBAL WP#/ACC STATUS (GWPACCS)<br>1 = $V_{CCQ}$+0.4V < WP#/ACC < 9.0V Detect, Operation Abort<br>0 = WP#/ACC OK | SR.3 does not provide a continuous indication of WP#/ACC level. The WSM interrogates and indicates the WP#/ACC level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when WP#/ACC≠$V_{ACCH}$. |
| SR.2 = GLOBAL (PAGE BUFFER) PROGRAM SUSPEND STATUS (GPBPSS)<br>1 = (Page Buffer) Program Suspended<br>0 = (Page Buffer) Program in Progress/Completed | SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status. |
| SR.1 = GLOBAL DEVICE PROTECT STATUS (GDPS)<br>1 = Erase or Program Attempted on a Locked Block, Operation Abort<br>0 = Unlocked | |
| SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R) | SR.0 is reserved for future use and should be masked out when polling the status register. |

Table 9.2. Status Register Definition (Continued)

| | NOTES: |
|---|---|
| SR.15 = GLOBAL WRITE STATE MACHINE STATUS (GWSMS)<br>1 = Ready<br>0 = Busy | Status Register SR.15-SR.9 indicates the status of the WSM.<br><br>Check SR.15 or RY/BY# to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.14 - SR.9 are invalid while SR.15="0". |
| SR.14 = GLOBAL BLOCK ERASE SUSPEND STATUS (GBESS)<br>1 = Block Erase Suspended<br>0 = Block Erase in Progress/Completed | |
| SR.13 = GLOBAL BLOCK ERASE AND FULL CHIP ERASE STATUS (GBEFCES)<br>1 = Error in Block Erase or Full Chip Erase<br>0 = Successful Block Erase or Full Chip Erase | If both SR.13 and SR.12 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit attempt, an improper command sequence was entered. |
| SR.12 = GLOBAL (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (GPBPOPS)<br>1 = Error in (Page Buffer) Program or OTP Program<br>0 = Successful (Page Buffer) Program or OTP Program | |
| SR.11 = GLOBAL WP#/ACC STATUS (GWPACCS)<br>1 = $V_{CCQ}$+0.4V < WPP#/ACC < 9.0V Detect, Operation Abort<br>0 = WP#/ACC OK | SR.11 does not provide a continuous indication of WP#/ACC level. The WSM interrogates and indicates the WP#/ACC level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.11 is not guaranteed to report accurate feedback when WP#/ACC≠$V_{ACCH}$. |
| SR.10 = GLOBAL (PAGE BUFFER) PROGRAM SUSPEND STATUS (GPBPSS)<br>1 = (Page Buffer) Program Suspended<br>0 = (Page Buffer) Program in Progress/Completed | |
| SR.9 = GLOBAL DEVICE PROTECT STATUS (GDPS)<br>1 = Erase or Program Attempted on a Locked Block, Operation Abort<br>0 = Unlocked | SR.9 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status. |
| SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R) | SR.8 is reserved for future use and should be masked out when polling the status register. |

Table 10. Extended Status Register Definition

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SMS | R | R | R | R | R | R | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

XSR.7 = STATE MACHINE STATUS (SMS)
1 = Page Buffer Program available
0 = Page Buffer Program not available

XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.

XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

# 1 Electrical Specifications

## 1.1 Absolute Maximum Ratings*

Operating Temperature

During Read, Erase and Program ...-40°C to +85°C (1)

Storage Temperature

During under Bias..... -40°C to +85°C

During non Bias..... -65°C to +125°C

Voltage On Any Pin (except $V_{CC}$, $V_{CCQ}$ and WP#/ACC)

.....-0.5V to $V_{CCQ}$+0.5V (2)

$V_{CC}$ and $V_{CCQ}$ Supply Voltage ..... -0.2V to +3.7V (2)

WP#/ACC Supply Voltage ..... -0.2V to +10.3V (2, 3, 4)

Output Short Circuit Current.....100mA (5)

**WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:

1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on $V_{CC}$, $V_{CCQ}$ and WP#/ACC pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is $V_{CC}$+0.5V which, during transitions, may overshoot to $V_{CC}$+2.0V for periods <20ns.
3. Maximum DC voltage on WP#/ACC may overshoot to +11.0V for periods <20ns.
4. WP#/ACC erase/program voltage is normally 2.7V-3.3V. Applying 9.0V-10.0V to WP#/ACC during erase/program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. WP#/ACC may be connected to 9.0V-10.0V for a total of 80 hours maximum.
5. Output shorted for no more than one second. No more than one output shorted at a time.

## 1.2 Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Operating Temperature | $T_A$ | -40 | +25 | +85 | °C | |
| $V_{CC}$ Supply Voltage | $V_{CC}$ | 2.7 | 3.0 | 3.3 | V | 1 |
| I/O Supply Voltage | $V_{CCQ}$ | 2.7 | 3.0 | 3.3 | V | 1 |
| WP#/ACC Voltage when Used as a Logic Control | $V_{IL}$ | -0.2 | | 0.4 | V | 1 |
| | $V_{IH}$ | 2.4 | | $V_{CCQ}$ + 0.4 | V | |
| WP#/ACC Supply Voltage | $V_{ACCH}$ | 9.0 | 9.5 | 10.0 | V | 1, 2 |
| Main Block Erase Cycling: WP#/ACC=$V_{IL}$ or $V_{IH}$ | | 100,000 | | | Cycles | |
| Parameter Block Erase Cycling: WP#/ACC=$V_{IL}$ or $V_{IH}$ | | 100,000 | | | Cycles | |
| Main Block Erase Cycling: WP#/ACC=$V_{ACCH}$, 80 hrs. | | | | 1,000 | Cycles | |
| Parameter Block Erase Cycling: WP#/ACC=$V_{ACCH}$, 80 hrs. | | | | 1,000 | Cycles | |
| Maximum WP#/ACC hours at $V_{ACCH}$ | | | | 80 | Hours | |

NOTES:

1. See DC Characteristics tables for voltage range-specific specification.
2. Applying WP#/ACC=9.0V-10.0V during a erase or program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. A permanent connection to WP#/ACC=9.0V-10.0V is not allowed and can cause damage to the device.

### 1.2.1 Capacitance (1) ($T_A$=+25°C, f=1MHz)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0.0V | | 4 | 7 | pF |
| WP#/ACC Input Capacitance | $C_{IN}$ | $V_{IN}$=0.0V | | 18 | 22 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$=0.0V | | 6 | 10 | pF |

NOTE:
1. Sampled, not 100% tested.

### 1.2.2 AC Input/Output Test Conditions

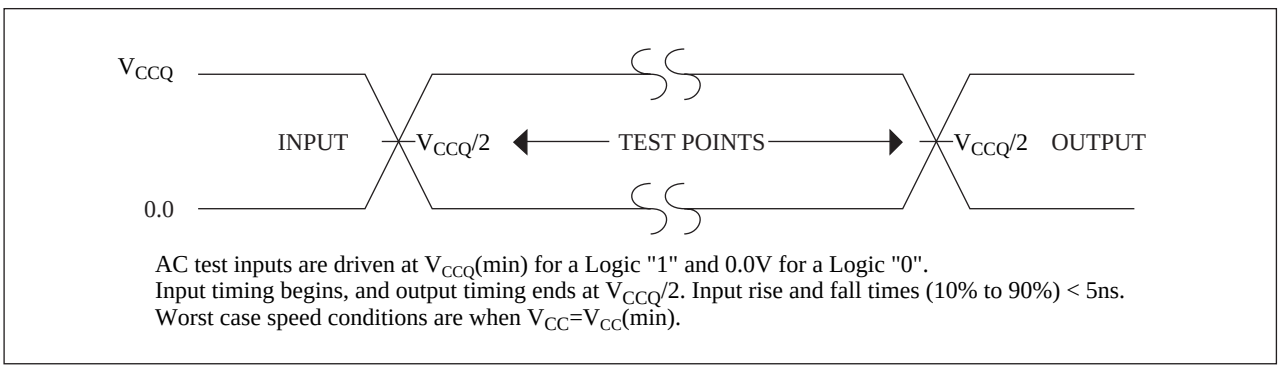



Figure 4. Transient Input/Output Reference Waveform for $V_{CC}$=2.7V-3.3V

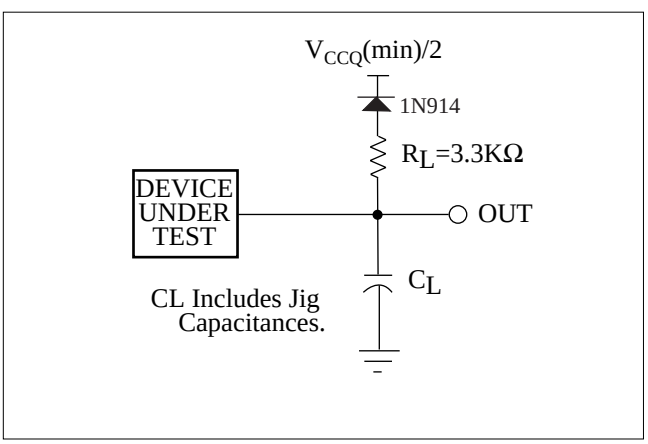



Figure 5. Transient Equivalent Testing Load Circuit

Table 11. Test Configuration Capacitance Loading Value

| Test Configuration | $C_L$ (pF) |
|---|---|
| $V_{CC}$=2.7V-3.3V | 50 |

### 1.2.3 DC Characteristics

$V_{CC}$=2.7V-3.3V

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | 1 | -1.0 | | +1.0 | µA | $V_{CC}$=$V_{CC}$Max., $V_{CCQ}$=$V_{CCQ}$Max., $V_{IN}$/$V_{OUT}$=$V_{CCQ}$ or GND |
| $I_{LO}$ | Output Leakage Current | 1 | -1.0 | | +1.0 | µA | |
| $I_{CCS}$ | $V_{CC}$ Standby Current | 1,7,8 | | 9 | 40 | µA | $V_{CC}$=$V_{CC}$Max., CE#=RST#= $V_{CCQ}$±0.2V, WP#/ACC=$V_{CCQ}$ or GND |
| $I_{CCAS}$ | $V_{CC}$ Automatic Power Savings Current | 1,3,7 | | 9 | 40 | µA | $V_{CC}$=$V_{CC}$Max., CE#=GND±0.2V, WP#/ACC=$V_{CCQ}$ or GND |
| $I_{CCD}$ | $V_{CC}$ Reset Current | 1,7 | | 9 | 40 | µA | RST#=GND±0.2V |
| $I_{CCR}$ | Average $V_{CC}$ Read Current Normal Mode | 1,6,7 | | 20 | 30 | mA | $V_{CC}$=$V_{CC}$Max., CE#=$V_{IL}$, OE#=$V_{IH}$, f=5MHz |
| | Average $V_{CC}$ Read Current Page Mode (8 Word Read) | 1,6,7 | | 5 | 10 | mA | |
| $I_{CCW}$ | $V_{CC}$ (Page Buffer) Program Current | 1,4,6,7 | | 20 | 60 | mA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,4,6,7 | | 10 | 20 | mA | WP#/ACC=$V_{ACCH}$ |
| $I_{CCE}$ | $V_{CC}$ Block Erase, Full Chip Erase Current | 1,4,6,7 | | 10 | 30 | mA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,4,6,7 | | 4 | 10 | mA | WP#/ACC=$V_{ACCH}$ |
| $I_{CCWS}$ $I_{CCES}$ | $V_{CC}$ (Page Buffer) Program or Block Erase Suspend Current | 1,2,6,7 | | 10 | 200 | µA | CE#=$V_{IH}$ |
| $I_{ACCS}$ $I_{ACCR}$ | WP#/ACC Standby or Read Current | 1,5,6,7 | | 2 | 5 | µA | WP#/ACC≤$V_{CC}$ |
| $I_{ACCW}$ | WP#/ACC (Page Buffer) Program Current | 1,4,5,6,7 | | 2 | 5 | µA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,4,5,6,7 | | 10 | 30 | mA | WP#/ACC=$V_{ACCH}$ |
| $I_{ACCE}$ | WP#/ACC Block Erase, Full Chip Erase Current | 1,4,5,6,7 | | 2 | 5 | µA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,4,5,6,7 | | 5 | 15 | mA | WP#/ACC=$V_{ACCH}$ |
| $I_{ACCWS}$ | WP#/ACC (Page Buffer) Program Suspend Current | 1,5,6,7 | | 2 | 5 | µA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,5,6,7 | | 10 | 200 | µA | WP#/ACC=$V_{ACCH}$ |
| $I_{ACCES}$ | WP#/ACC Block Erase Suspend Current | 1,5,6,7 | | 2 | 5 | µA | WP#/ACC=$V_{IL}$ or $V_{IH}$ |
| | | 1,5,6,7 | | 10 | 200 | µA | WP#/ACC=$V_{ACCH}$ |

DC Characteristics (Continued)

$V_{CC}$=2.7V-3.3V

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | 5 | -0.4 | | 0.4 | V | |
| $V_{IH}$ | Input High Voltage | 4 | 2.4 | | $V_{CCQ}$ + 0.4 | V | |
| $V_{OL}$ | Output Low Voltage | 4,8 | | | 0.2 | V | $V_{CC}$=$V_{CC}$Min., $V_{CCQ}$=$V_{CCQ}$Min., $I_{OL}$=100µA |
| $V_{OH}$ | Output High Voltage | 4 | $V_{CCQ}$ -0.2 | | | V | $V_{CC}$=$V_{CC}$Min., $V_{CCQ}$=$V_{CCQ}$Min., $I_{OH}$=-100µA |
| $V_{ACCH}$ | WP#/ACC during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations | 5 | 9.0 | 9.5 | 10.0 | V | |
| $V_{LKO}$ | $V_{CC}$ Lockout Voltage | | 1.5 | | | V | |

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values are the reference values at $V_{CC}$=3.0V, $V_{CCQ}$=3.0V and $T_A$=+25°C unless $V_{CC}$ is specified.
2. $I_{CCWS}$ and $I_{CCES}$ are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of $I_{CCES}$ and $I_{CCR}$ or $I_{CCW}$. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of $I_{CCWS}$ and $I_{CCR}$.
3. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings ($t_{AVQV}$) provide new data when addresses are changed.
4. Sampled, not 100% tested.
5. Applying 9.5V±0.5V to WP#/ACC provides fast erasing or fast programming mode. In this mode, WP#/ACC is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the $V_{CC}$ power bus.
   Applying 9.5V±0.5V to WP#/ACC during erase/program can only be done for a maximum of 1,000 cycles on each block. WP#/ACC may be connected to 9.5V±0.5V for a total of 80 hours maximum.
6. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.
7. For all pins other than those shown in test conditions, input level is $V_{CCQ}$ or GND.
8. Includes RY/BY#.

### 1.2.4 AC Characteristics - Read-Only Operations(1)

$V_{CC}$=2.7V-3.3V, $T_A$=-40°C to +85°C

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{AVAV}$ | Read Cycle Time | | 75 | | ns |
| $t_{AVQV}$ | Address to Output Delay | | | 75 | ns |
| $t_{ELQV}$ | CE# to Output Delay | 3 | | 75 | ns |
| $t_{APA}$ | Page Address Access Time | | | 25 | ns |
| $t_{GLQV}$ | OE# to Output Delay | 3 | | 20 | ns |
| $t_{PHQV}$ | RST# High to Output Delay | | | 150 | ns |
| $t_{EHQZ}$, $t_{GHQZ}$ | CE# or OE# to Output in High Z, Whichever Occurs First | 2 | | 20 | ns |
| $t_{ELQX}$ | CE# to Output in Low Z | 2 | 0 | | ns |
| $t_{GLQX}$ | OE# to Output in Low Z | 2 | 0 | | ns |
| $t_{OH}$ | Output Hold from First Occurring Address, CE# or OE# change | 2 | 0 | | ns |
| $t_{AVEL}$, $t_{AVGL}$ | Address Setup to CE#, OE# Going Low for Reading Status Register | 4, 6 | 10 | | ns |
| $t_{ELAX}$, $t_{GLAX}$ | Address Hold from CE#, OE# Going Low for Reading Status Register | 5, 6 | 10 | | ns |
| $t_{EHEL}$, $t_{GHGL}$ | CE#, OE# Pulse Width High for Reading Status Register | 6 | 20 | | ns |

NOTES:
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact to $t_{ELQV}$.
4. Address setup time ($t_{AVEL}$, $t_{AVGL}$) is defined from the falling edge of CE# or OE# (whichever goes low last).
5. Address hold time ($t_{ELAX}$, $t_{GLAX}$) is defined from the falling edge of CE# or OE# (whichever goes low last).
6. Specifications $t_{AVEL}$, $t_{AVGL}$, $t_{ELAX}$, $t_{GLAX}$ and $t_{EHEL}$, $t_{GHGL}$ for read operations apply to only status register read operations.

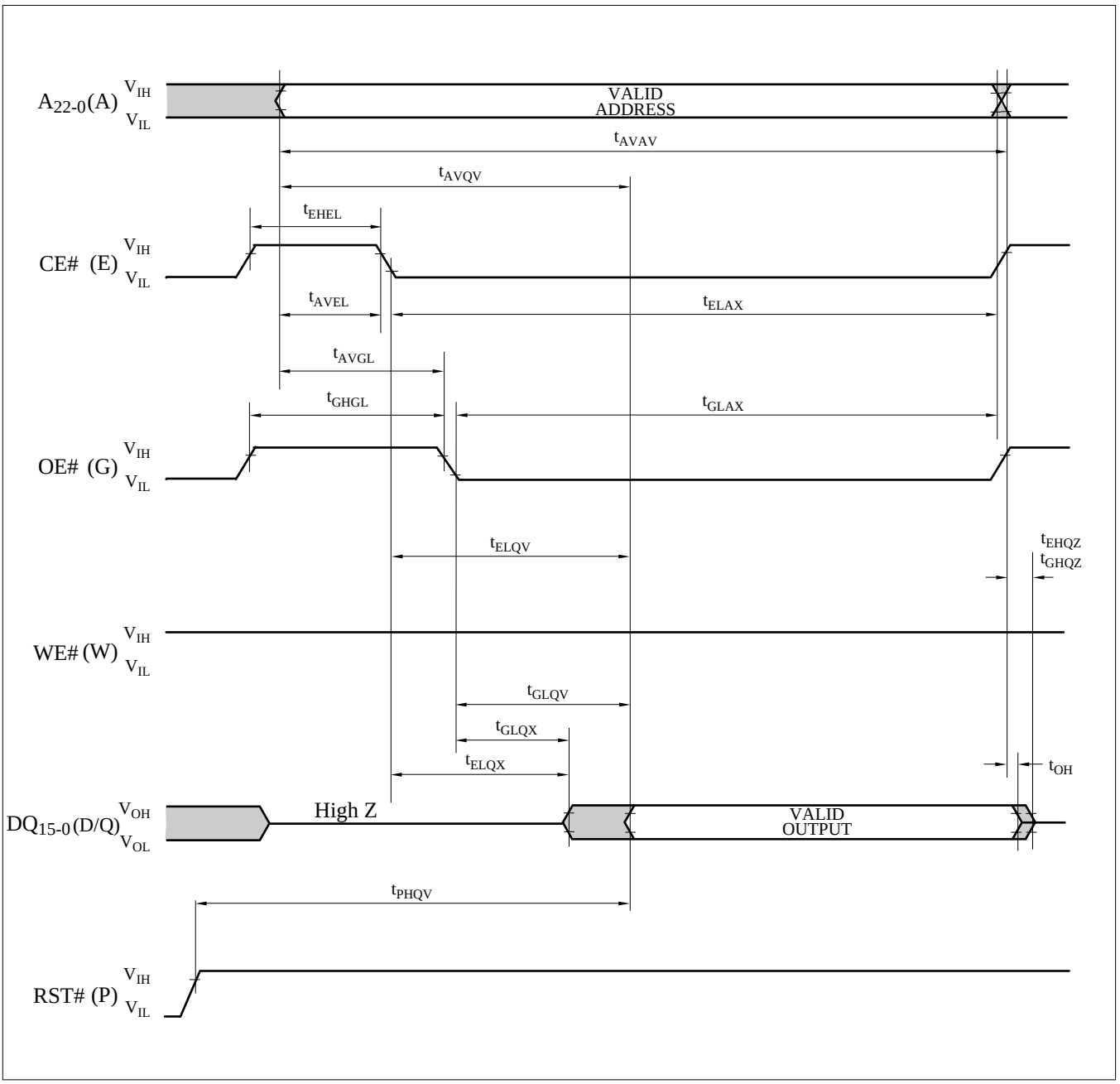



Figure 6. AC Waveform for Single Asynchronous Read Operations
from Status Register, Identifier Codes, OTP Block or Query Code

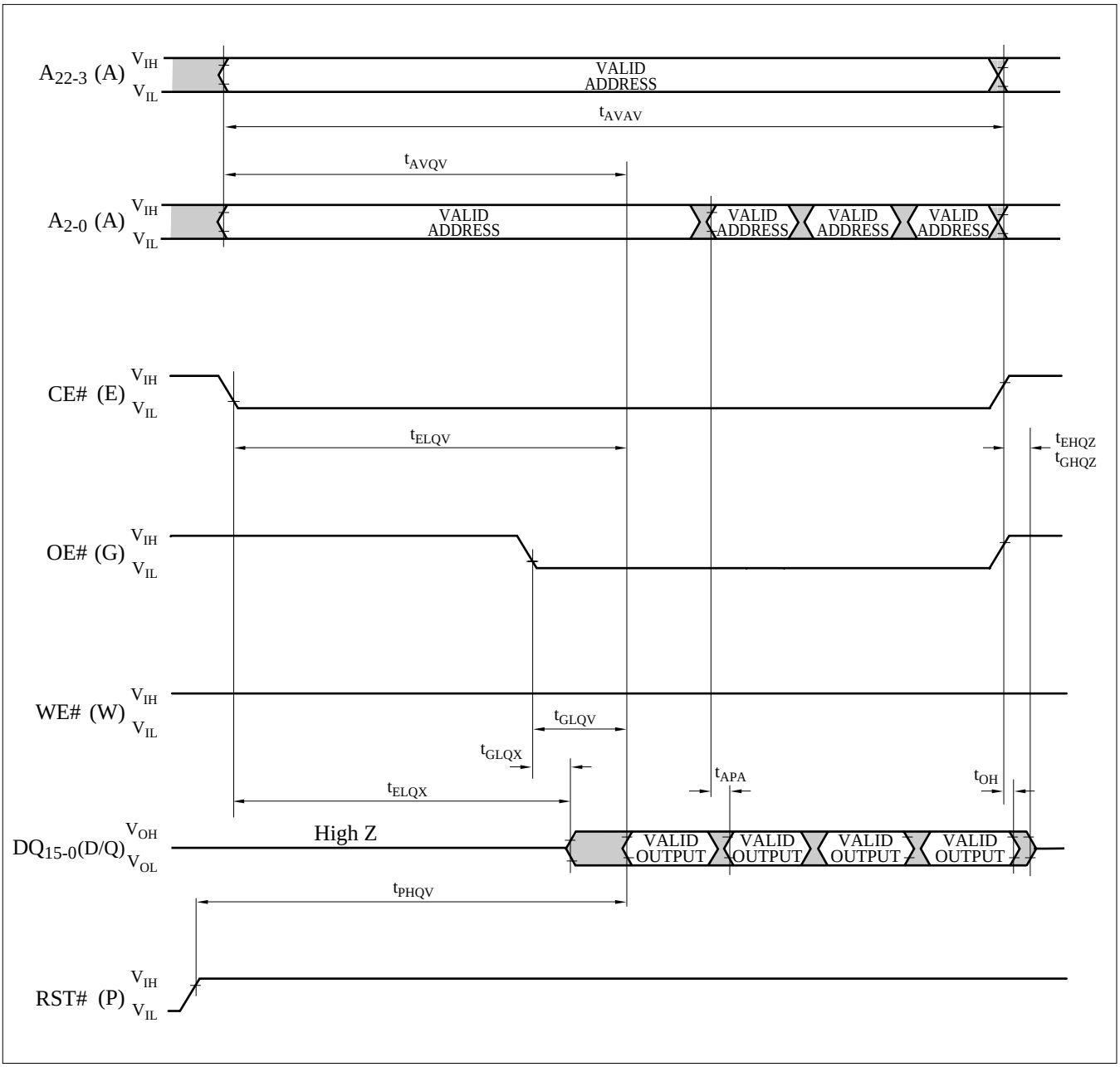



Figure 7. AC Waveform for Asynchronous 4-Word Page Mode
Read Operations from Main Blocks or Parameter Blocks

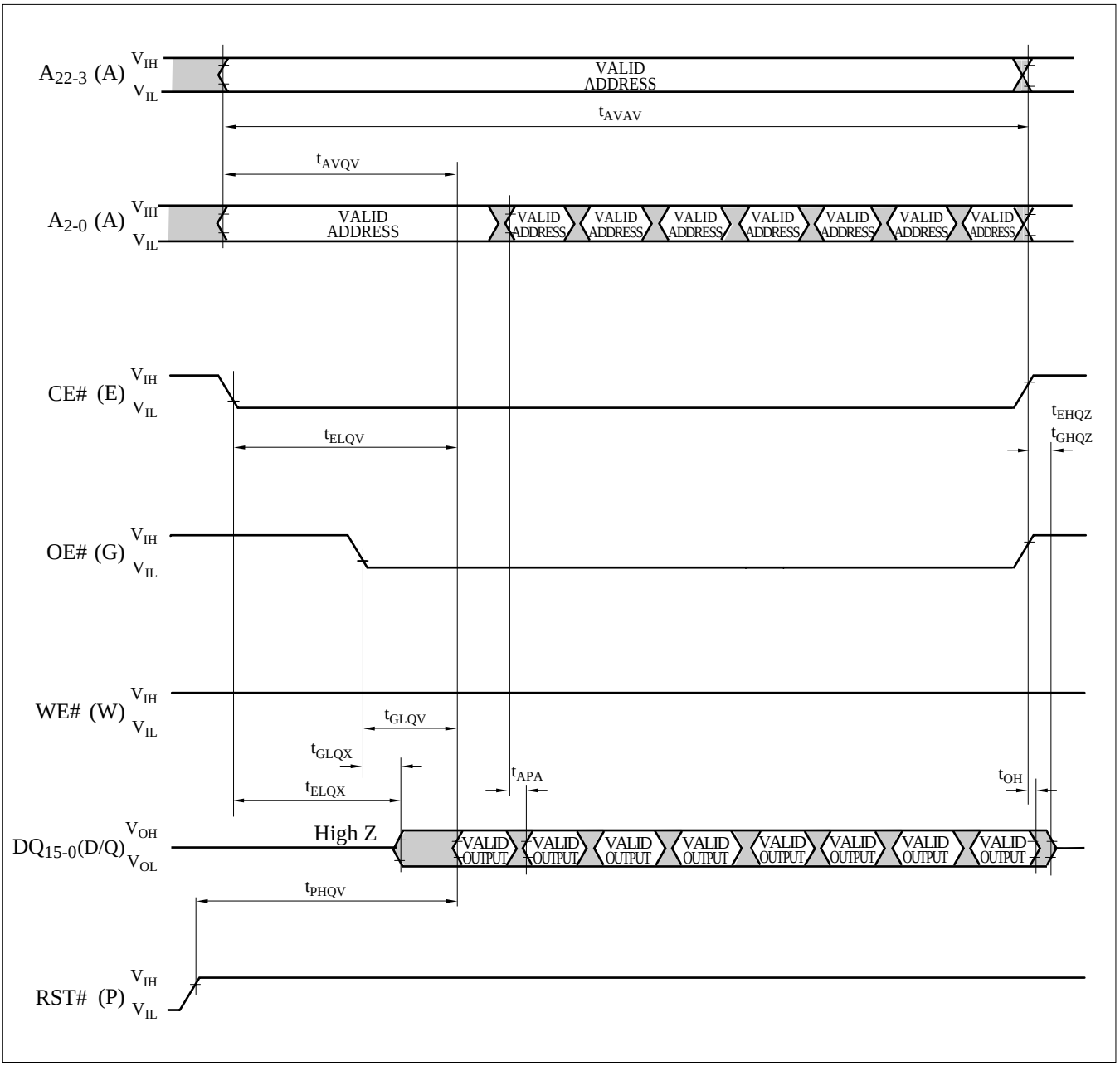


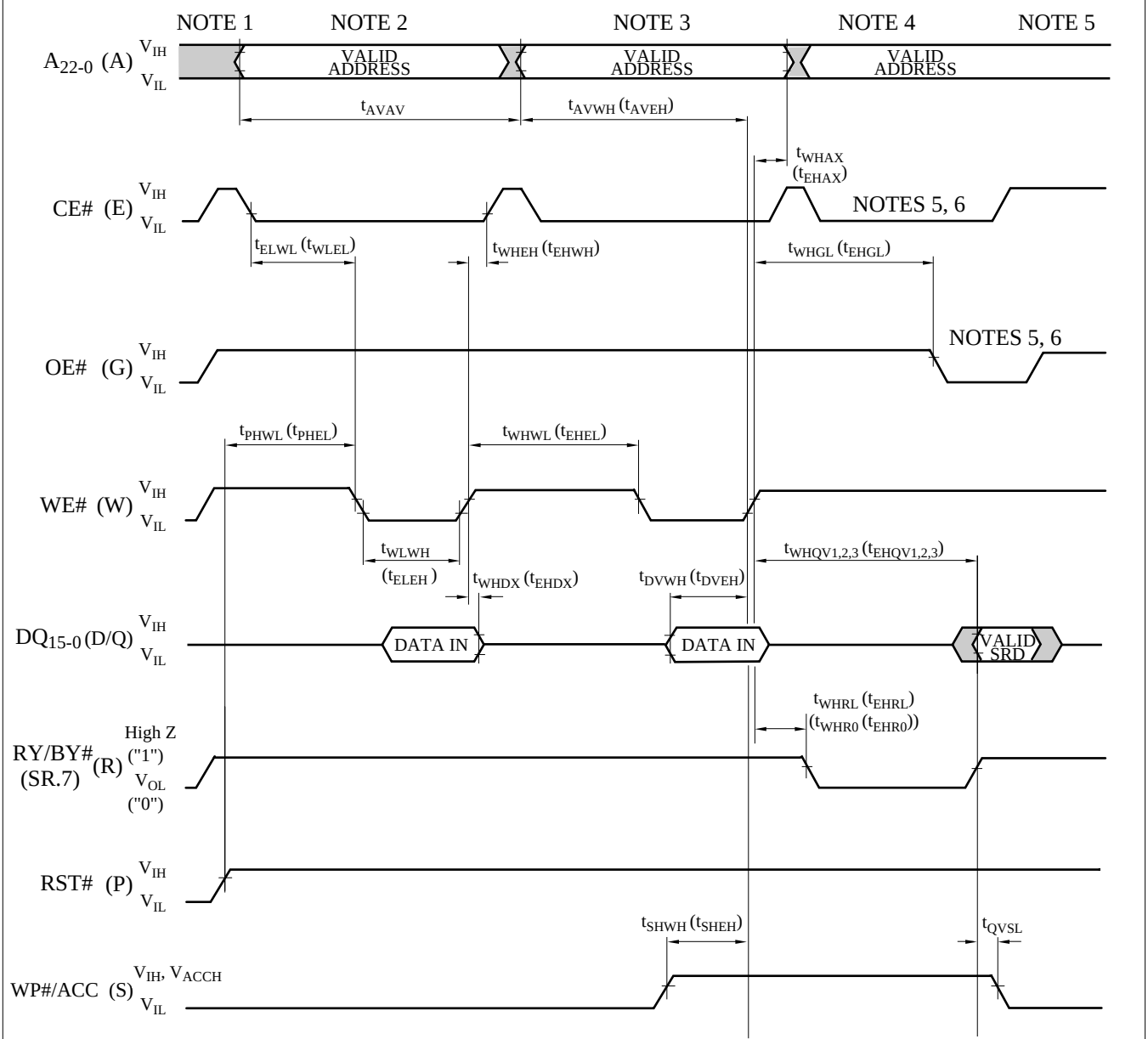

Figure 8. AC Waveform for Asynchronous 8-Word Page Mode
Read Operations from Main Blocks or Parameter Blocks

### 1.2.5 AC Characteristics - Write Operations[1, 2]

$V_{CC}$=2.7V-3.3V, $T_A$=-40°C to +85°C

| Symbol | Parameter | | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{AVAV}$ | Write Cycle Time | | | 75 | | ns |
| $t_{PHWL}$ ($t_{PHEL}$) | RST# High Recovery to WE# (CE#) Going Low | | 3 | 150 | | ns |
| $t_{ELWL}$ ($t_{WLEL}$) | CE# (WE#) Setup to WE# (CE#) Going Low | | | 0 | | ns |
| $t_{WLWH}$ ($t_{ELEH}$) | WE# (CE#) Pulse Width | | 4 | 50 | | ns |
| $t_{DVWH}$ ($t_{DVEH}$) | Data Setup to WE# (CE#) Going High | | 7 | 40 | | ns |
| $t_{AVWH}$ ($t_{AVEH}$) | Address Setup to WE# (CE#) Going High | | 7 | 40 | | ns |
| $t_{WHEH}$ ($t_{EHWH}$) | CE# (WE#) Hold from WE# (CE#) High | | | 0 | | ns |
| $t_{WHDX}$ ($t_{EHDX}$) | Data Hold from WE# (CE#) High | | | 0 | | ns |
| $t_{WHAX}$ ($t_{EHAX}$) | Address Hold from WE# (CE#) High | | | 0 | | ns |
| $t_{WHWL}$ ($t_{EHEL}$) | WE# (CE#) Pulse Width High | | 5 | 25 | | ns |
| $t_{SHWH}$ ($t_{SHEH}$) | WP#/ACC High Setup to WE# (CE#) Going High | WP#/ACC=$V_{IH}$ | 3 | 0 | | ns |
| | | WP#/ACC=$V_{ACCH}$ | | 200 | | |
| $t_{WHGL}$ ($t_{EHGL}$) | Write Recovery before Read | | | 30 | | ns |
| $t_{QVSL}$ | WP#/ACC High Hold from Valid SRD, RY/BY# High Z | | 3 | 0 | | ns |
| $t_{WHR0}$ ($t_{EHR0}$) | WE# (CE#) High to SR.7 Going "0" | | 3, 6 | | $t_{AVQV}$ +50 | ns |
| $t_{WHRL}$ ($t_{EHRL}$) | WE# (CE#) High to RY/BY# Going Low | | 3 | | 100 | ns |

NOTES:
1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width ($t_{WP}$) is defined from the falling edge of CE# or WE# (whichever goes low last) to the rising edge of CE# or WE# (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$.
5. Write pulse width high ($t_{WPH}$) is defined from the rising edge of CE# or WE# (whichever goes high first) to the falling edge of CE# or WE# (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. $t_{WHR0}$ ($t_{EHR0}$) after the Read Query or Read Identifier Codes/OTP command=$t_{AVQV}$+100ns.
7. Refer to Table 5 for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.




NOTES:
1. $V_{CC}$ power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, OE# and CE# must be driven active, and WE# de-asserted.

Figure 9. AC Waveform for Write Operations

### 1.2.6 Reset Operations

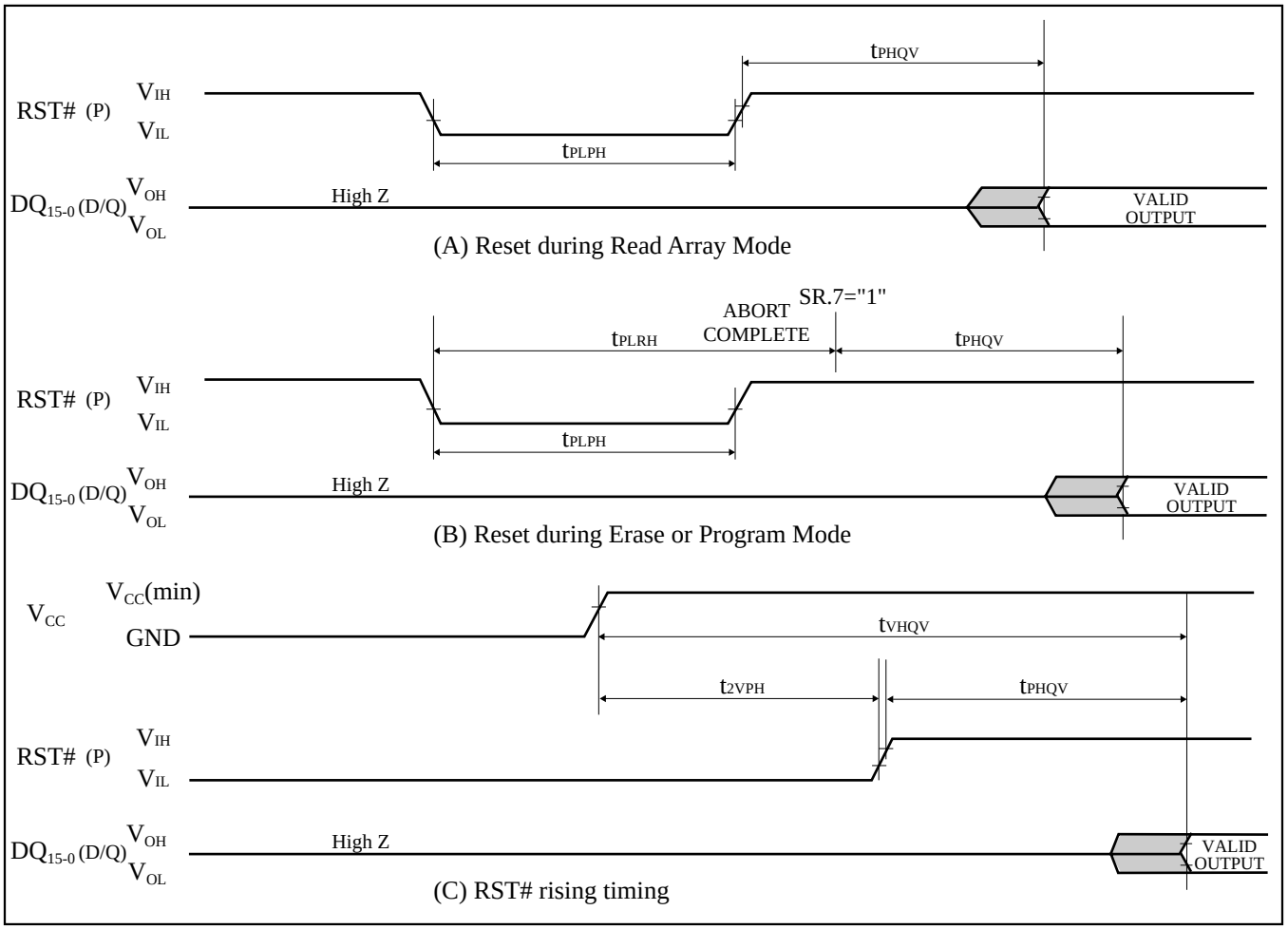



Figure 10. AC Waveform for Reset Operations

Reset AC Specifications ($V_{CC}$=2.7V-3.3V, $T_A$=-40°C to +85°C)

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{PLPH}$ | RST# Low to Reset during Read<br>(RST# should be low during power-up.) | 1, 2, 3 | 100 | | ns |
| $t_{PLRH}$ | RST# Low to Reset during Erase or Program | 1, 3, 4 | | 22 | µs |
| $t_{2VPH}$ | $V_{CC}$ 2.7V to RST# High | 1, 3, 5 | 100 | | ns |
| $t_{VHQV}$ | $V_{CC}$ 2.7V to Output Delay | 3 | | 1 | ms |

NOTES:
1. A reset time, $t_{PHQV}$, is required from the later of SR.7 (RY/BY#) going "1" (High Z) or RST# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for $t_{PHQV}$.
2. $t_{PLPH}$ is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If RST# asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding RST# low minimum 100ns is required after $V_{CC}$ has been in predefined range and also has been in stable there.

### 1.2.7 Block Erase, Full Chip Erase, (Page Buffer) Program and OTP Program Performance(3)

$V_{CC}$=2.7V-3.3V, $T_A$=-40°C to +85°C

| Symbol | Parameter | Notes | Page Buffer Command is Used or not Used | WP#/ACC=$V_{IL}$ or $V_{IH}$ (In System) | | | WP#/ACC=$V_{ACCH}$ (In Manufacturing) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ.(1) | Max.(2) | Min. | Typ.(1) | Max.(2) | |
| $t_{WPB}$ | 4-Kword Parameter Block Program Time | 2 | Not Used | | 0.05 | 0.3 | | 0.04 | 0.12 | s |
| | | 2 | Used | | 0.03 | 0.12 | | 0.02 | 0.06 | s |
| $t_{WMB}$ | 32-Kword Main Block Program Time | 2 | Not Used | | 0.38 | 2.4 | | 0.31 | 1.0 | s |
| | | 2 | Used | | 0.24 | 1.0 | | 0.17 | 0.5 | s |
| $t_{WHQV1}$/ $t_{EHQV1}$ | Word Program Time | 2 | Not Used | | 11 | 200 | | 9 | 185 | µs |
| | | 2 | Used | | 7 | 100 | | 5 | 90 | µs |
| $t_{WHOV1}$/ $t_{EHOV1}$ | OTP Program Time | 2 | Not Used | | 36 | 400 | | 27 | 185 | µs |
| $t_{WHQV2}$/ $t_{EHQV2}$ | 4-Kword Parameter Block Erase Time | 2 | - | | 0.5 | 4 | | 0.4 | 4 | s |
| $t_{WHQV3}$/ $t_{EHQV3}$ | 32-Kword Main Block Erase Time | 2 | - | | 0.9 | 5 | | 0.8 | 5 | s |
| | Full Chip Erase Time | 2 | | | 240 | 1400 | | 200 | 1400 | s |
| $t_{WHRH1}$/ $t_{EHRH1}$ | (Page Buffer) Program Suspend Latency Time to Read | 4 | - | | 5 | 10 | | 5 | 10 | µs |
| $t_{WHRH2}$/ $t_{EHRH2}$ | Block Erase Suspend Latency Time to Read | 4 | - | | 5 | 20 | | 5 | 20 | µs |
| $t_{ERES}$ | Latency Time from Block Erase Resume Command to Block Erase Suspend Command | 5 | - | 500 | | | 500 | | | µs |

NOTES:
1. Typical values measured at $V_{CC}$=3.0V, WP#/ACC=3.0V or 9.5V, and $T_A$=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (WE# or CE# going high) until SR.7 going "1" or RY/BY# going High Z.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than $t_{ERES}$ and its sequence is repeated, the block erase operation may not be finished.

## A-1 RECOMMENDED OPERATING CONDITIONS

### A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

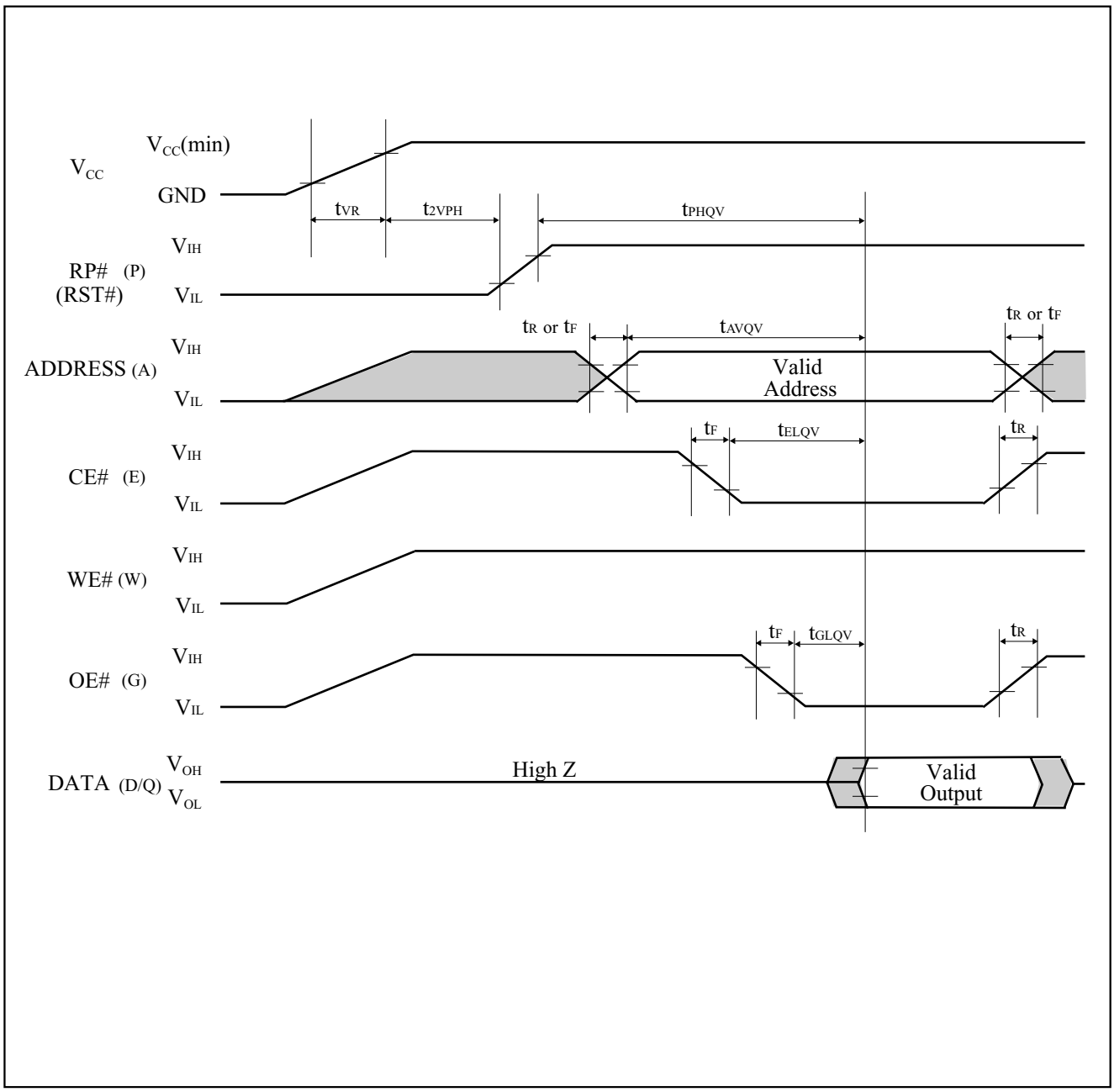



Figure A-1. AC Timing at Device Power-Up

For the AC specifications $t_{VR}$, $t_R$, $t_F$ in the figure, refer to the next page. See the “ELECTRICAL SPECIFICATIONS“ described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

### A-1.1.1 Rise and Fall Time

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{VR}$ | $V_{CC}$ Rise Time | 1 | 0.5 | 30000 | µs/V |
| $t_R$ | Input Signal Rise Time | 1, 2 | | 1 | µs/V |
| $t_F$ | Input Signal Fall Time | 1, 2 | | 1 | µs/V |

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

## A-1.2 Glitch Noises

Do not input the glitch noises which are below $V_{IH}$ (Min.) or above $V_{IL}$ (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

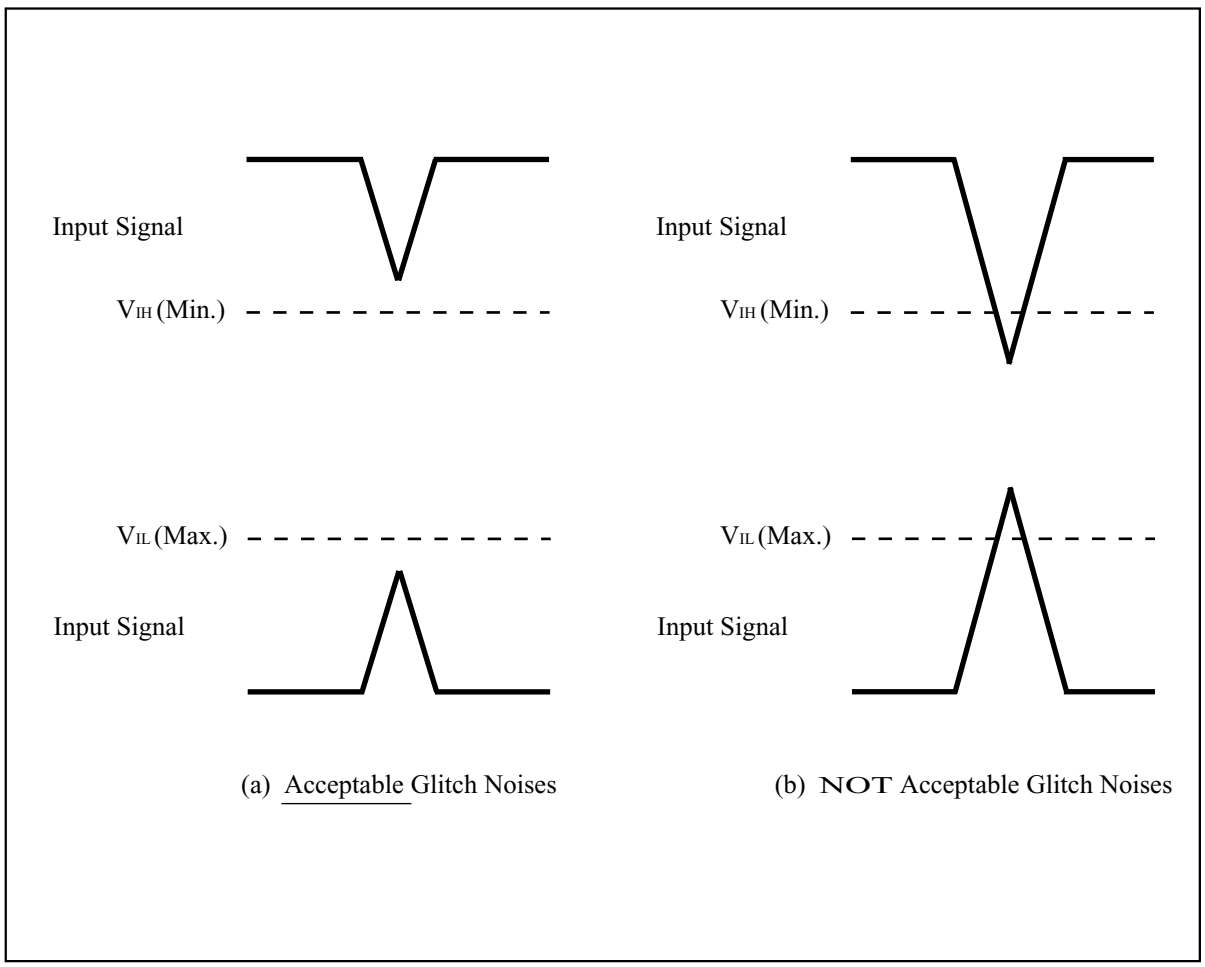



Figure A-2. Waveform for Glitch Noises

See the “DC CHARACTERISTICS“ described in specifications for $V_{IH}$ (Min.) and $V_{IL}$ (Max.).

## A-2 RELATED DOCUMENT INFORMATION(1)

| Document No. | Document Name |
|---|---|
| AP-001-SD-E | Flash Memory Family Software Drivers |
| AP-006-PT-E | Data Protection Method of SHARP Flash Memory |
| AP-007-SW-E | RP#, $V_{PP}$ Electric Potential Switching Circuit |

NOTE:
1. International customers should contact their local SHARP or distribution sales office.

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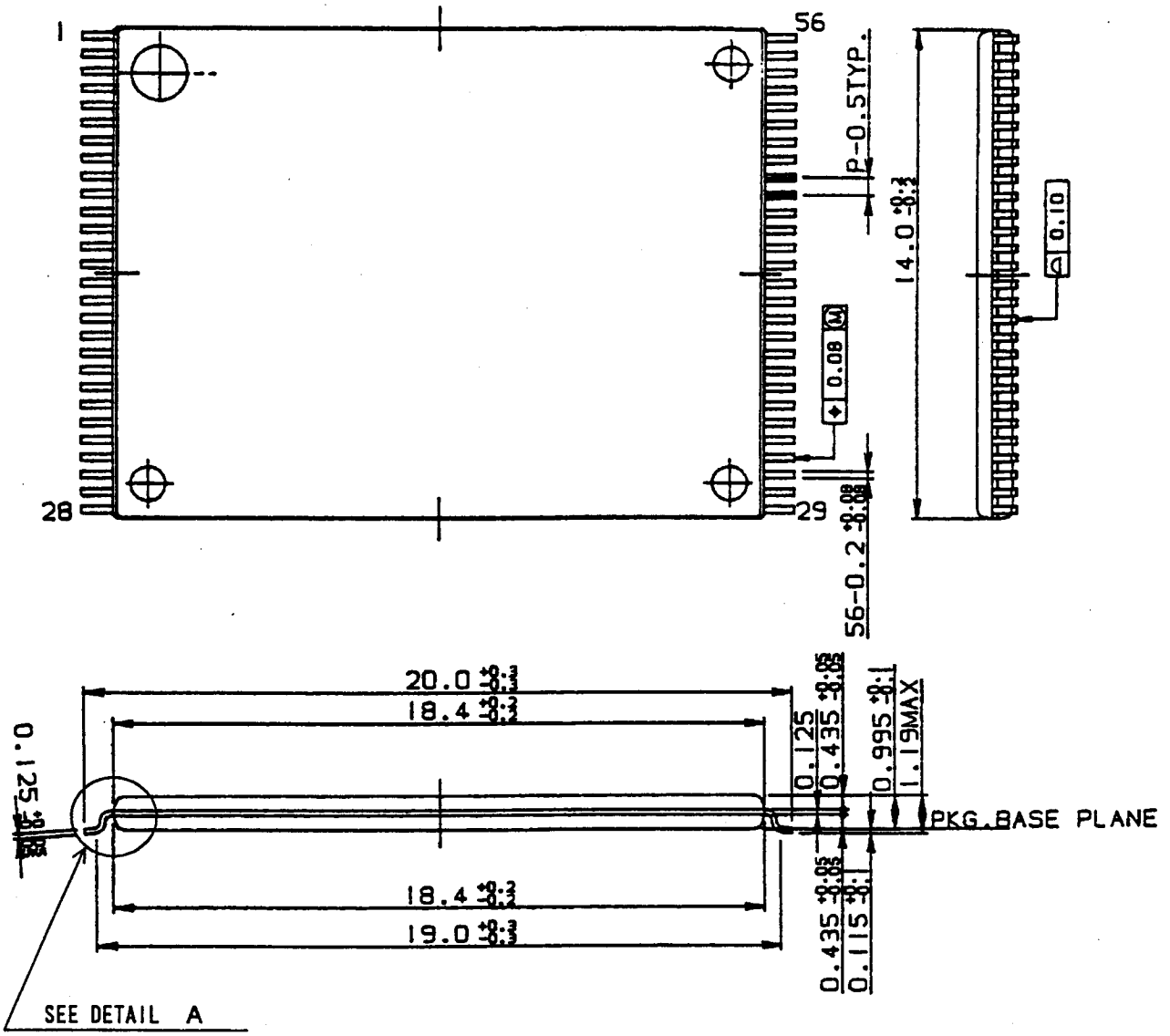


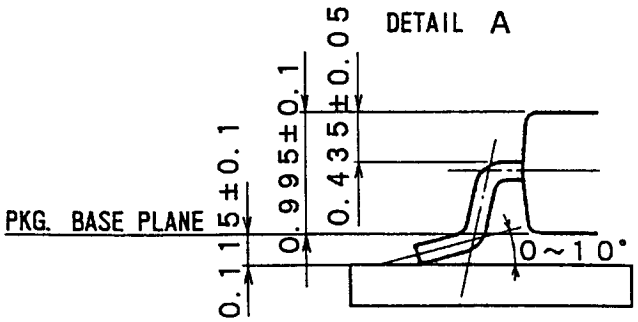


| | | | |
|---|---|---|---|
| 名称 NAME | TSOP56-P-1420 | リード仕上 LEAD FINISH | TIN-LEAD PLATING |
| DRAWING NO. | AA1115 | 単位 UNIT | mm |

備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。
NOTE Plastic body dimensions do not include burr of resin.

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